REMARKS

Claim 13 has been added. Claims 1-13 are pending in the present application. Claim 13 is newly added. Support for claim 13 can be found, *inter alia*, in the objected claim 4. Claims 3 and 12 have been amended to improve readability. Claims 1 and 8 are independent.

Initially, Applicants thank the Examiner for recognizing the novelty claims 4, 5, 7, and 8-11.

Rejections Under 35 U.S.C. § 112

Claim 3 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Applicants respectfully traverse.

Applicants assert that the rejection is now moot given the amendment to claims 3 and 12. Accordingly, Applicants respectfully request that the Examiner withdraw the 35 U.S.C. § 112, second paragraph, rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1 and 2 are rejected under 35 U.S.C. § 102(e) as being anticipated by Guinea et al. (U.S. Patent No. 6,414,526) in view of Ahuja (U.S. Patent No. 5,307,381). Applicants respectfully traverse.

With regard to claim 1, Applicants assert that Guinea et al. fail to disclose a plurality of sampling modules concurrently receiving a second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells, as recited in claim 1. Referring to FIG. 2 of Guinea et al.,

the Examiner suggests that a first pulse signal is the input to the delay line 1 and that a second pulse signal is CK_{in} which provides a signal to sampling circuit 3. Applicants assert that FIG. 2 clearly and plainly shows that the input signal to the delay line 1 and the sampling circuit 3 is the same signal, CKin. Guinea et al. only discloses one input signal, CKin and does not disclose a first pulse and a second pulse. Therefore, Guinea et al. cannot disclose a plurality of sampling modules concurrently receiving a second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells, as recited in claim 1.

Further, the Examiner admits that Guinea et al. does not disclose a conditioning circuit that receives a clock signal and outputs a first pulse signal and a second pulse signal. To make up for the deficiencies of the Guinea et al. reference, the Examiner provides an Ahuja reference. Ahuja is directed to skew-free clock signal distribution network in a microprocessor. Ahuja discloses a clock signal that is converted to a global clock signal that is synchronized for use by a plurality of devices. Applicants assert that a same global clock signal that is used by a plurality of devices is not the same as a first pulse and a second pulse. Therefore, Ahuja cannot disclose a plurality of sampling modules concurrently receiving a second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells, as recited in claim 1.

Moreover, Applicants assert that there is no motivation to combine the Guinea et al. reference with the Ahuja reference. The Examiner asserts that the motivation to combine is "eliminating the clock skew in a clock signal distribution network of the apparatus" (page 4 of the outstanding Office Action).

Applicants respectfully submit that the only way Guinea et al. and Ahuja could be combined is by utilizing Applicant's disclosure as a blueprint, which is not permitted. C.R. Bard, Inc. v. M3 Systems, Inc., 48 USPQ2d 1225 (Fed. Cir. 1998); Interconnect Planning Corp. v. Feio, 227 USPQ 543 (Fed. Cir. 1985); In re Rouffet, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).

The CAFC has stated that the best defense against the subtle but powerful attraction of a hind sight-based obviousness analysis is rigorous application of the requirement for showing of the teaching or motivation to combine prior art references. In re Dembiczak, 50 USPQ2d 1614 (Fed. Cir. 1999). Evidence of a suggestion, teaching or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or in some cases, from the nature of the problem to be solved. Dembiczak, at 1617.

The Prior Art References Themselves

Applicants point out that, according to Guinea et al. at Col. 1, lines 23-33, a clock signal distribution network is:

> . . . typically accomplished by coupling a clock input signal of a microprocessor chip to a global driver circuit. The global driver circuit then couples the clock signal to various units of the microprocessor via a plurality of clock distribution lines. One disadvantage associated with this prior clock signal distribution network in the microprocessor chip is that the clock signal distribution network introduces different delays to the clock signal (i.e., clock skew).

Applicants submit that there is no mention of a clock skew problem in Guinea et al. Moreover, there is shown in FIG. 2 only a CKin clock signal that is an input to the delay line 1 and the sampling circuit 3. What is not shown in Guinea et al. is any clock signal distribution network, where a clock signal distribution network includes a global driver circuit according to

Ahuja. There is no clock signal distribution network in Guinea et al. from which to cause skew. Therefore, there cannot possibly be a motivation to combine Guinea et al. and Ahuja that includes the elimination of a clock skew in a clock signal distribution network of the apparatus, as suggested by the examiner.

Nature of the Problem to be Solved

Applicants respectfully submit that the problem being solved in Guinea et al. is providing a reliable delayed locked loop (DLL). Guinea et al. does this, referring to FIG. 2, by subjecting a clock signal CKin to a delay and controlling the delay so that the clock signal is delayed by a specific amount and the clock signal is output as CKout.

The problem to be solved by Ahuja is to receive a clock input and generate global clock signals that are synchronized among a plurality of devices.

Combining the system of Guinea et al. with the system of Ahuja would break the system of Guinea et al. such that Guinea et al. could not provide a reliable DLL. The Examiner suggests that the Ahuja device could be inserted into the system of Guinea et al. as shown in FIG. 2. In doing so, the Ahuja device would receive the CKin signal, generate a global clock signal, and output the same global output signal to the delay device 1 and the sampling circuit 3. The problem with this construction is that the DLL device of Guinea et al. would be applying a delay to the global clock signal and not to the input clock signal CKin. Moreover, there is no disclosure of any fixed time that it may take for CKin to propagate through the system of Ahuja. Thus, setting CKin to be delayed to a specific amount would be absolutely impossible under the combination suggested by the Examiner, since there is no known CKin input to the Guinea et al. system. Without a known CKin input to the Guinea et al. system, the Guinea et al. system could not provide a specific delay to CKin and could not function as intended.

Knowledge of One of Ordinary Skill in the Art

As suggested in Dembiczak, the final source for suggestion, teaching or motivation could be the knowledge of one of ordinary skill in the art. Regardless of the source, the Examiner is still required to provide actual evidence. It must be based on specific, objective evidence of record. In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. Broad denials and conclusory statements are not sufficient to establish a genuine issue of material fact. Dembiczak at 1617.

The Examiner asserts that one of ordinary skill in the art would have modified Guinea et al. as taught by Ahuja in order to improve "eliminating the clock skew in a clock signal distribution network of the apparatus". (page 4 of the outstanding Office Action). However, as discussed above, there is no signal distribution network, as defined by Ahuja, in Guinea et al. to cause a clock skew problem. Moreover, there is no disclosure of a clock skew problem in Guinea et al.

Accordingly, Applicant respectfully submits that one of ordinary skill in the art would not have been motivated to modify Guinea et al. in view of the teachings of Ahuja based on either the Examiner's asserted motivation based on the Examiner's broad conclusory statement that doing so would eliminate the clock skew in a clock signal distribution network of an apparatus, where no clock signal distribution network is present.

Since the Examiner has failed to establish a proper motivation, either from the references themselves, by virtue of the nature of the problem being solved by the references, or by knowledge of one of ordinary skill in the art, Applicant respectfully submits that the Examiner has failed to establish a proper *prima facie* case of obviousness.

Applicants respectfully request that the art grounds of rejection be withdrawn.

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Guinea et al. in view of Ahuja and in further view of the admitted prior art, Fig. 2, in the present application. Applicants respectfully traverse.

As discussed above, Guinea et al. in view of Ahuja do not disclose a plurality of sampling modules concurrently receiving a second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells as recited in claim 1.

Fig. 2 of the specification, shows a tapped delay circuit that connects to a multiplexer. The sampling modules in Fig. 2 are not shown or described as concurrently receiving a second pulse. Therefore, Fig. 2 cannot teach or suggest a plurality of sampling modules concurrently receiving a second pulse as input, each sampling module receiving said second pulse signal as input while said first pulse signal propagates through said tapped delay circuit, each sampling module being clocked by a tapped output signal from one of said plurality of tapped delay cells, as recited in claim 1. Claim 1 is therefore not rendered obvious to one skilled in the art by Lee et al. in view of the prior art of Fig. 2.

With regard to claim 6, Applicants assert that claim 6 is allowable at least because it depends from independent claim 1 which Applicants have shown to be allowable.

Accordingly, Applicants respectfully request that the art grounds of rejection be withdrawn.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-12 are patentable over the relied upon references, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any outstanding matters remain pending in this application, Applicants request that the Examiner contact the undersigned to discuss such matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

John A. Castellano
Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/RFS:ewd